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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,713	06/26/2003	Naysen Jesse Robertson	200208055-1	5776

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EXAMINER	
BARAN, MARY C	

ART UNIT	PAPER NUMBER
2857	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/606,713	ROBERTSON ET AL.	
	Examiner	Art Unit	
	Mary C. Baran	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-20 and 22-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8-20 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The action is responsive to the Amendment filed on 20 June 2007. Claims 1, 2, 4-6, 8-20 and 22-31 are pending. Claims 1, 20 and 25 are amended. Claims 3, 7 and 21 are cancelled. Claims 30 and 31 are new.

2. The amendments filed 20 June 2007 are sufficient to overcome the 35 U.S.C. 101 rejections.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-6, 8-20 and 22-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley (U.S. Patent No. 6,617,872) in view of Hawkins et al. (U.S. PG-Pub. No. US2003/0130969) (hereinafter Hawkins).

Referring to claim 1, Vogley teaches a margin testing system for frequency margin testing an electronic system (see Vogley, column 4 lines 1-2), the margin testing system comprising:

a controller (see Vogley, column 4 lines 39-43);

and a digital frequency synthesizer configured to generate one or more test frequencies (see Vogley, column 3 lines 17-43 and column 4 lines 39-43) for application to one or more of a plurality of components of said electronic system (see Vogley, column 2 lines 57-64 and Figure 1) in response to commands from said controller (see Vogley, column 4 lines 39-51 and column 6 lines 15-20);

wherein said controller is configured to monitor a response of the plurality of components (see Vogley, column 2 lines 57-64 and Figure 1) of said electronic system to said test frequencies (see Vogley, column 4 lines 23-51), and

wherein the plurality of components are operably connected within said electronic system such that no invasive connection is necessary to apply the one or more test frequencies (see Vogley, column 2 lines 57-61).

Vogley does not specify that the microprocessor (i.e. controller) is a baseboard management controller.

Hawkins teaches a baseboard management controller which provides autonomous monitoring, event logging and recovery control (see Hawkins, page 2 [0015]-[0017]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because substituting a baseboard management controller in place of the microprocessor, or controller, would have allowed the skilled artisan to provide intelligence to the platform management (see Hawkins, page 2 paragraph [0015]).

Referring to claim 2, Vogley teaches collecting and analyzing data regarding a response of one or more selected components of said system to said test frequencies (see Vogley, column 3 lines 17-32).

Referring to claims 4 and 5, Vogley teaches a hardware monitor configured to communicate with said controller and said frequency synthesizer to measure values of said one or more test frequencies and to transmit said measured values to said controller (see Vogley, column 4 lines 39-51 and column 5 lines 1-19) and to receive data regarding response of said components to said one or more test frequencies (see Vogley, column 4 lines 39-51 and column 5 lines 1-19).

Referring to claim 6, Vogley teaches that said controller is configured to transmit command signals to said frequency synthesizer to cause the synthesizer to generate said one or more test frequencies (see Vogley, column 5 lines 1-19 and column 6 lines 15-20).

Referring to claims 8-10, Vogley teaches all the features of the claimed invention except that the BMC implements Intelligent Platform Management Interface (IPMI) protocol; that the communication bus is a I^2C-based bus; that said I^2C-based bus is an IPMB bus; and that said computer system is a computer server.

Hawkins teaches that the BMC implements Intelligent Platform Management Interface (IPMI) protocol (see Hawkins, pages 1-2 [0014]); that the communication bus

is an I^2C-based bus (see Hawkins, page 1 [0006]); that said I^2C-based bus is an IPMB bus (see Hawkins, page 1 [0013]); and that said computer system is a computer server (see Hawkins, page 1 [0004]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because implementing an Intelligent Platform Management Interface (IPMI) protocol, including an I^2C-based bus, wherein said I^2C-based bus is an IPMB bus, and that said computer system is a computer server would have allowed the skilled artisan to provide a star intelligent platform management bus topology.

Referring to claim 11, Vogley teaches that said frequency synthesizer receives an input reference clock signal and, in response to a command signal from said controller, generates an output clock signal as a multiple of said input clock signal (see Vogley, column 3 lines 7-16).

Referring to claim 12, Vogley teaches that said frequency synthesizer applies said output clock signal as a test frequency to one or more components for frequency margin testing thereof (see Vogley, column 3 lines 7-16).

Referring to claim 13, Vogley teaches that said frequency synthesizer generates each one of a plurality of test frequencies based on a pattern of input bits received from the controller (see Vogley, column 6 lines 15-37).

Referring to claim 14, Vogley teaches that said controller initiates margin testing in response to commands from an external system (see Vogley, Figure 1 and column 3 lines 17-20).

Referring to claim 15, Vogley teaches that said external system comprises: a console in communication with said controller via a serial bus (see Vogley, column 3 lines 7-16).

Referring to claims 16 and 17, Vogley teaches that external system comprises: a remote computer in communication with said controller, said remote computer communicates with said controller via a network-based connection (see Vogley, column 4 lines 44-67).

Referring to claim 18, Vogley teaches that sad external system includes a scripting entity for generating commands for transmission to said controller (see Vogley, column 3 lines 34-43).

Referring to claim 19, Vogley teaches that said one or more components receive nominal clock frequencies in the absence of said test frequencies (see Vogley, column 6 lines 48-61).

Referring to claim 20, Vogley teaches a computer system comprising:

a processor (see Vogley, Figure 1);

a plurality of components in communication with said processor for performing a plurality of tasks (see Vogley, Figure 1 "test device 24,25");

a controller (see Vogley, column 4 lines 39-43);

and a digital frequency synthesizer configured to generate one or more test frequencies (see Vogley, column 3 lines 17-43 and column 4 lines 39-43) for application to selected ones of said plurality of components for frequency margin testing thereof (see Vogley, column 2 lines 57-64 and Figure 1) in response to commands from said controller (see Vogley, column 4 lines 39-51 and column 6 lines 15-20);

wherein said controller is configured to monitor a response of said plurality of components (see Vogley, column 2 lines 57-64 and Figure 1) of said electronic system to said one or more test frequencies (see Vogley, column 4 lines 23-51), and

wherein the plurality of components are operably connected within said electronic system such that no invasive connection is necessary to apply the one or more test frequencies (see Vogley, column 2 lines 57-61).

Vogley does not specify that the microprocessor (i.e. controller) is a baseboard management controller.

Hawkins teaches a baseboard management controller which provides autonomous monitoring, event logging and recovery control (see Hawkins, page 2 [0015]-[0017]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because substituting a baseboard management controller in place of the microprocessor, or controller, would have allowed the skilled artisan to provide intelligence to the platform management (see Hawkins, page 2 paragraph [0015]).

Referring to claims 22-24, Vogley teaches all the features of the claimed invention except that the BMC implements Intelligent Platform Management Interface (IPMI) protocol; that the communication bus is a I^2C-based bus; that said I^2C-based bus is an IPMB bus; and that said computer system is a computer server.

Hawkins teaches that the BMC implements Intelligent Platform Management Interface (IPMI) protocol (see Hawkins, pages 1-2 [0014]); that the communication bus is an I^2C-based bus (see Hawkins, page 1 [0006]); that said I^2C-based bus is an IPMB bus (see Hawkins, page 1 [0013]); and that said computer system is a computer server (see Hawkins, page 1 [0004]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because implementing an Intelligent Platform Management Interface (IPMI) protocol, including an I^2C-based bus, wherein said I^2C-based bus is an IPMB bus, and that said computer system is a computer server would have allowed the skilled artisan to provide a star intelligent platform management bus topology.

Referring to claim 25, Vogley teaches a method for frequency margin testing of one or more components of a computer system, comprising a controller and a digital frequency synthesizer, in communication with said controller (see Vogley, column 4 lines 1-2), comprising:

transmitting, by the controller, one or more commands to said synthesizer for said frequency margin testing (see Vogley, column 4 lines 39-51 and column 6 lines 15-20);

generating, by the synthesizer, one or more test frequencies (see Vogley column 3 lines 17-43 and column 4 lines 39-43) for application to said one or more components (see Vogley, column 2 lines 57-63 and Figure 1);

monitoring, by the controller, a response of said one or more of components (see Vogley, column 2 lines 57-64 and Figure 1) of said computer system to said test frequencies (see Vogley, column 4 lines 23-51); and

storing the response as a test result (see Vogley, column 5 lines 13-16);

wherein the plurality of components are operably connected within said electronic system such that no invasive connection is necessary to apply the one or more test frequencies (see Vogley, column 2 lines 57-61).

Vogley does not specify that the microprocessor (i.e. controller) is a baseboard management controller.

Hawkins teaches a baseboard management controller which provides autonomous monitoring, event logging and recovery control (see Hawkins, page 2 [0015]-[0017]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because substituting a baseboard management controller in place of the microprocessor, or controller, would have allowed the skilled artisan to provide intelligence to the platform management (see Hawkins, page 2 paragraph [0015]).

Referring to claim 26, Vogley teaches collecting and analyzing data regarding a response of one or more selected components of said system to said test frequencies (see Vogley, column 3 lines 17-32).

Referring to claims 27 and 28, Vogley teaches all the features of the claimed invention except that the BMC implements Intelligent Platform Management Interface (IPMI) protocol; that the communication bus is a I^2C-based bus; that said I^2C-based bus is an IPMB bus; and that said computer system is a computer server.

Hawkins teaches that the BMC implements Intelligent Platform Management Interface (IPMI) protocol (see Hawkins, pages 1-2 [0014]); that the communication bus is an I^2C-based bus (see Hawkins, page 1 [0006]); that said I^2C-based bus is an IPMB bus (see Hawkins, page 1 [0013]); and that said computer system is a computer server (see Hawkins, page 1 [0004]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because implementing an Intelligent Platform Management Interface (IPMI) protocol, including an

I^2C-based bus, wherein said I^2C-based bus is an IPMB bus, and that said computer system is a computer server would have allowed the skilled artisan to provide a star intelligent platform management bus topology.

Referring to claim 29, Vogley teaches that said frequency synthesizer generates each one of a plurality of test frequencies based on a pattern of input bits received from the controller (see Vogley, column 6 lines 15-37).

Referring to claim 30, Vogley teaches all the features of the claimed invention except transmitting, by the baseband management controller, one or more further commands to said synthesizer for said frequency margin testing of the same component of said one or more components when the stored test result is a failed test result.

Hawkins teaches transmitting, by the baseband management controller, one or more further commands to said synthesizer for said frequency margin testing of the same component of said one or more components when the stored test result is a failed test result (see Hawkins, page 1 [0013]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because storing a failed test result would have allowed the skilled artisan to examine the error later and alert without the aid of run-time software (see Hawkins, page 1 [0013]).

Referring to claim 31, Vogley teaches all the features of the claimed invention except transmitting, by the baseband management controller, one or more further commands to said synthesizer for said frequency margin testing of another component of said one or more component when the stored test result is a successful test result.

Hawkins teaches transmitting, by the baseband management controller, one or more further commands to said synthesizer for said frequency margin testing of another component of said one or more component when the stored test result is a successful test result.(see Hawkins, page 2 [0017]).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Vogley to include the teachings of Hawkins because storing a successful test result would have allowed the skilled artisan to ensure that the system is functioning correctly.

Response to Arguments

4. Applicant's arguments filed 16 January 2007 have been fully considered but they are not persuasive.

Applicant argues that Vogley does not teach that the "plurality of components are operably connected within said electronic system such that no invasive connection is necessary to apply the one or more test frequencies." However, Applicant's arguments are not well taken. Vogley teaches that the integrated circuit devices (i.e. components) are plugged into test sockets mounted on the side of the test handler board (see Vogley, column 2 lines 57-61). This procedure is not invasive to either the integrated

circuit devices (i.e. components), because no probes or sensors are physically inserted into integrated circuit devices. Therefore, Vogley teaches that the plurality of components are operably connected within said electronic system such that no invasive connection is necessary to apply the one or more test frequencies (see Vogley, column 2 lines 57-61).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Baran whose telephone number is (571) 272-2211. The examiner can normally be reached on Monday to Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mary Catherine Baran
3 September 2007